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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,121	02/12/2002	Alois Biebl	02075/TL	7724

7590 03/16/2004

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/074,121	Applicant(s) BIEBL, ALOIS	
	Examiner Prabodh M Dharia	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02-12-2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-09-2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 09-09-2002 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because there is no English translation of references or no English abstract. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

3. The information disclosure statement filed 09-09-2002 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because total word count exceeds 150.

Correction is required. See MPEP § 608.01(b).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,400,101 in view of Claims 1-7, of U.S. Patent No. 6,515,434 B1.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

a drive circuit for an LED array which comprises a first LED cluster (40) and at least one second LED cluster (42; 44), a switch (SI, S2, S3)being arranged in series with each LED cluster (40, 42,44), and each LEI) cluster (40, 42, 44) having a supply terminal via which it can be connected to a supply voltage it being possible to drive each switch (SI, S2,S3) so as to permit a current flow in the associated LEE) cluster, having a control loop (46) which is designed to drive the switch (SI) of the first LED cluster (40) so as to achieve a constant mean value of the current (I_{LED}) flowing through the first LLD cluster (40), the control loop (46) being designed to drive at least one switch (S2, S3) of a second LED cluster (42,44), characterized in that the drive circuit further comprises: a total current detection device with the (R_{Mess}) with the aid of which it is possible to determine an actual magnitude (U_{Mess}) which corresponds to the sum of the currents through at least two, in particular through all of the second LED cluster (42,44), and a comparison unit (50, 50a) in which the actual magnitude (U_{mess}) can be compared with a prescribable desired magnitude (U_{OL}).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kennedy et al. (5,634,711).

Regarding Claim 1, Kennedy et al. teaches a drive circuit for an LED array (Col. 5, Lines 13,14) which comprises a first LED cluster (40) (Col. 5, Line33,34) and at least one second LED cluster (42; 44) (Col. 5, Lines 33,34), a switch (SI, S2, S3) being arranged in series with each LED cluster (40, 42,44), (Col. 5, line 14-16) and each LED cluster (40, 42, 44) having a supply terminal via which it can be connected to a supply voltage (Col. 5, Lines 49-53) it being possible to drive each switch (SI, S2,S3) (Col. 5, Lines 49-59) so as to permit a current flow in the associated LED cluster, having a control loop (46) which is designed to drive the switch (SI) of the first LED cluster (40) so as to achieve a constant mean value of the current (I_{LED}) flowing through the first LED cluster (40) (Col. 5, Line 49 to Col. 6, line 3, Col. 6, Line 51 to Col. 7, Line 12, Col. 7, Lines 20-30), the control loop (46) being designed to drive at least one switch (S2, S3) of a second LED cluster (42,44) (Col. 6, Line 51 to col. 7, Line 12), characterized in that the drive circuit further comprises: a total current detection device with the (R_{Mess}) with the aid of which it is possible to determine an actual magnitude (U_{Mess}) which corresponds to the sum of the currents through at least two, in particular through all of the second LED cluster (42,44), (Col. 6, Lines 5-50) and a comparison unit (50, 50a) in which the actual magnitude (U_{mess}) can be compared with a prescribable desired magnitude (U_{OL}) (Col. 6, Lines 5-50, Col. 7, Line 66 to Col. 8, Line 13, Col. 8, Line 49 to Col. 10, Line7).

Regarding Claim 2, Kennedy et al. teaches the desired magnitude (U_{OL}) can be set by a user (Col. 6, Lines 31-40).

Regarding Claim 3, Kennedy et al. teaches the comparison unit (50, 50a) is designed to output an information signal (78) in the event of undershooting of the desired magnitude (U_{OL}) by the actual magnitude (U_{Mess}) (Col. 7, Lines 48-56).

Regarding Claim 4, Kennedy et al. teaches comprises a monitoring unit (50, 50b), with which the current flow through the first LED cluster (40) can be monitored (Col. 6, Lines 4-24).

Regarding Claim 5, Kennedy et al. teaches the monitoring unit (50, 50h) is designed in such a way that the control loop (46) is disconnected when a current flow which is outside a prescribable tolerance range is determined in the first LED cluster (40) (Col. 6, Lines 4-34).

Regarding Claim 6, Kennedy et al. teaches the monitoring unit (50, 50b) is designed in such a way that the first LED cluster (40) is disconnected when a current flow 20 which is outside a prescribable tolerance range is determined in the first LED cluster (40), and a second LED cluster (42, 44) is made relative to the first LED cluster (Col. 6, Lines 4-50).

Regarding Claim 7, Kennedy et al. teaches comprises an undervoltage detection device (64) which is designed to output an undervoltage warning signal (76) when the supply voltage

(U_{Batt}) falls below a prescribable value (U_{Refl}) (Col. 6, Lines 22, 23, Lines 41-50, Col. 7, Lines 48-56).

Regarding Claim 8, Kennedy et al. teaches the prescribable value (U_{Refl}) is equal to or greater than the sum of the forward voltages of all the LEDs of an LED cluster(40, 42, 44) (Col. 5, Lines 49-59, Col. 6, Lines 18-21, Lines 39-41).

Regarding Claim 9, Kennedy et al. teaches the prescribable value (U_{Refl}) can be set manually or can be prescribed permanently (Col. 6, Lines 34-40, Col. 6, Lines 18-21).

Regarding Claim 10, Kennedy et al. teaches comprises an output unit (50, 50c, ST1) to which the information signal (78) and/or the undervoltage, warning signal (76) can be transmitted (Col. 7, Lines 31-67, Col. 6, Lines 4-24).

Regarding Claim 11, Kennedy et al. teaches the output unit (50, 50c,ST1) comprises at least one transistor (ST1) which is located in an open collector circuit and whose base is connected to the comparison unit (50a) for is the purpose of transmitting the information signal (78), and/or is connected to the undervoltage detection device (64) for the purpose of transmitting the undervoltage warning signal (76) (Col.7, Lines 31-67, Col. 6, Lines 22-24).

Regarding Claim 12, Kennedy et al. teaches comprises a closing delay device (74), which is designed to deactivate the output unit (50, 50c, STI) for a predetermined time after the closure of the drive circuit (Col. 9, Line 49 to Col.10, Line 7).

Regarding Claim 13, Kennedy et al. teaches the output unit (50, 50c, ST1) comprises a flip-flop (88), the base of the of the transistor (ST1) being connected to the output of the flip-flop (88), and the set input (S) of the flip-flop (88) being connected to the undervoltage detection device (64) in order to transmit the undervoltage warning signal (76), and/or being connected to the comparison unit (50a) in order, to transmit the information signal (78) (figure 4, Col. 7, Lines 1-30, Col. 9, Line 49 to Col.10, Line 7).

Regarding Claim 14, Kennedy et al. teaches the closing delay device (74) is designed to apply a closing delay signal (80) to the reset input (R) of the flip--flop (88) of the output unit (50, 50c, ST1) over the duration of the closing delay (Col. 6, Lines 1-30, the delay generated by wave form generator, Col. 9, lines 49 to Col. 10, Line 7).

Regarding Claim 15, Kennedy et al. teaches the actual magnitude (U_{Mess}) corresponds to a time average value of the sum of the currents through at least two, in particular through all of the second LED clusters (42, 44) (Col. 6, Lines 31-40).

Regarding Claim 16, Kennedy et al. teaches a drive circuit for an LED array (Col. 5, Lines 13,14) which comprises a first LED cluster (40) (Col. 5, Line 33,34) and at least one

second LED cluster (42; 44) (Col. 5, Lines 33,34), a switch (SI, S2, S3) being arranged in series with each LED cluster (40, 42,44), (Col. 5, line 14-16) and each LED cluster (40, 42, 44) having a supply terminal via which it can be connected to a supply voltage (Col. 5, Lines 49-53) comprising the following steps: a) driving the switch (Sl) of the first LED cluster (40) with a drive signal (CLK) (Col. 5, lines 41-48) so as to achieve a constant mean value of the current (LED) flowing through the first LED cluster (40), and driving at least one second LED cluster (42, 44) with the same drive signal (CLK), (Col. 5, Line 49 to Col. 6, line 3, Col. 6, Line 51 to Col. 7, Line 12, Col. 7, Lines 20-30), b) measuring an actual magnitude which corresponds to the sum of the currents through at least two, in particular through all of the second LED clusters (42, 44) , (Col. 6, Lines 5-50) and c) comparing the actual magnitude with a prescribable desired magnitude (U_{OL}) (Col. 6, Lines 5-50, Col. 7, Line 66 to Col. 8, Line 13, Col. 8, Line 49 to Col. 10, Line7).

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references either anticipate or render the claims obvious. In order to not to be repetitive and exhaustive, the examiner did draft additional rejection based on those references.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Michael et al. (6,433,483 B1) Jewellery Illumination.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2673

February 11,2004

VIJAY SHANKAR
PRIMARY EXAMINER